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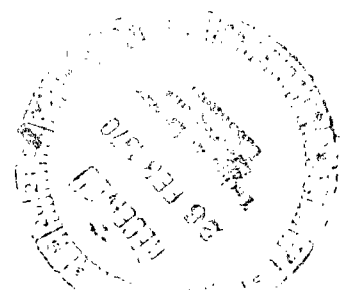
DESIGN ANALYSIS AND PERFORMANCE OF A 2.5 kVA PULSE-WIDTH-MODULATED STATIC INVERTER

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Cleveland, Ohio

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • FEBRUARY 1970

1. Report No. NASA TN D-5586	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle DESIGN ANALYSIS AND PERFORMANCE OF A 2.5 kVA PULSE-WIDTH-MODULATED STATIC INVERTER		5. Report Date February 1970
		6. Performing Organization Code
7. Author(s) Francis Gourash and Arthur G. Birchenough		8. Performing Organization Report No. E-5262
9. Performing Organization Name and Address Lewis Research Center National Aeronautics and Space Administration Cleveland, Ohio 44135		10. Work Unit No. 120-27
		11. Contract or Grant No.
		13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Washington, D.C. 20545		Technical Note
		14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

Performance and circuit design analyses of an experimental pulse-width-modulated dc to 400-Hz three-phase ac inverter provide basic design information. The inverter is rated for an output of 2.5 kVA and uses parallel-connected power transistors with balancing reactors for equal current sharing and auxiliary circuits to provide fast switching and compensation for the finite switching times. The measured efficiency of the power stage is 86 percent with a unity-power-factor load of 1.5 kW, and 77.5 percent at the 2.5 kVA, 0.7 power factor, full-load rating. Total harmonic distortion of the sinusoidal output voltage is 6.5 percent.

17. Key Words (Suggested by Author(s)) Power conditioning High frequency Static inverter High power Pulse width modulation Light weight	18. Distribution Statement Unclassified - unlimited		
19. Security Classif. (of this report) Unclassified	20. Security Classif. (of this page) Unclassified	21. No. of Pages 32	22. Price* $3.00

*For sale by the Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151

DESIGN ANALYSIS AND PERFORMANCE OF A 2.5 kVA

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SUMMARY

The circuits and performance of an experimental pulse-width-modulated dc-to-ac static inverter are described and presented as design information. The inverter operates at a carrier frequency of 7.2 kilohertz and produces a sinusoidal 400-hertz three-phase output of 120/208 volts. Paralleled power transistors with current balancing reactors in a half-bridge circuit provide an output of 2.5 kilovolt-amperes. Delayed turnon and fast turnoff circuits minimize current spikes because of the transistors' finite switching times. The inverter was tested with a laboratory power supply providing the high dc voltage required by the inverter and therefore the output voltage for these tests was not regulated.

The performance tests demonstrated that pulse width modulation (PWM) is feasible for dc-to-ac static inverters, and they showed that the paralleled transistors switched effectively at the high frequency rate with equal load current sharing. The principal advantage of PWM is that only a small filter is required for a low-distortion sinusoidal output voltage because the low-frequency harmonics are small and the high frequencies are easily filtered. The peak efficiency of the power stages is 86 percent at a power output of 1.5 kilowatts (power factor, PF = 1.0) and 77.5 percent at 2.5 kilovolt-amperes (PF = 0.7). Circuit analysis indicates that the efficiency can be improved with refinements to the logic and power transistor drive circuits. The ac output voltage can be regulated from no load to full load by controlling the inverter dc input voltage to ±20 percent of a nominal value of 185 volts. The power losses, size, weight, and criticality of adjustment to the control circuits can be minimized by the use of integrated circuits.

INTRODUCTION

Pulse width modulation (PWM) has been shown to provide a larger static inverter weight reduction than other techniques which synthesize sinusoidal voltages by various

combinations of square wave voltages (refs. 1 and 2). This weight advantage was first recognized in an inverter optimization study which resulted in a conceptual design of a high power, transformerless, three-phase, PWM inverter (ref. 3). An experimental model of this conceptual design was developed and fabricated by TRW Equipment Laboratories under NASA contract NAS 3-6475 to prove its feasibility. But the design and performance of this model are only partially reported in the literature because unresolved problems in the converter stage prevented final testing and evaluation (ref. 4).

The converter stage raises the level of the dc input voltage to the high voltage required by the inverter. Since this is an auxiliary function, only the high voltage dc-to-ac inverter stage of the experimental model was tested at the Lewis Research Center with a laboratory power supply in place of the converter stage. The circuit design and the analysis of the performance data from these tests are presented because the circuits and performance of the dc-to-ac inverter stage of this experimental model are considered fundamental to the PWM technique. The circuits and performance data also provide a design basis for future PWM inverters of advanced designs.

The experimental inverter model is rated for 2.5 kilovolt-amperes and produces a sinusoidal three-phase output voltage of 120 to 208 volts at 400 hertz. The PWM inverter stage operates with a carrier frequency of 7.2 kilohertz, and the power transistors switching at this frequency are paralleled to obtain the current rating.

A brief description of the PWM technique and a complete description of the design and operation of the circuits of the experimental inverter model are given. The tests are described and the results are analyzed from which conclusions are drawn concerning the feasibility and performance of the inverter stage. The schematic circuit drawing and a list of the component parts of the inverter are presented in figures 21 to 23 at the back of the report.

PULSE-WIDTH-MODULATION PRINCIPLES AND OPERATION

Pulse width modulation (PWM) is basically a sampling technique in which a modulating waveform, whose frequency corresponds to the desired output frequency, is periodically sampled at a high frequency rate. The sampling frequency is generally much higher than the frequency of the modulating waveform and usually of a ratio of the order of 20:1. The purpose of this sampling is to produce a train of pulses with constant amplitudes but with variable pulse widths. The width of each pulse is proportional to the amplitude of the modulating wave during the sampling interval in which it was formed. The pulse train is raised to a usable power level by a power amplifier and then an amplified modulating waveform is recovered at the output by passing the pulse train through a low-pass filter circuit. The advantage of this technique is that a small lightweight filter can be used. This is possible because the frequencies to be removed

from the pulse train are considerably higher than the fundamental frequency of the modulating wave and are easily attenuated in a small filter.

A fundamental method of producing the PWM waveform signal for static inverters is illustrated in figure 1. The modulating wave is the low frequency sine wave of frequency f_m (fig. 1(a)), and the high frequency sawtooth sweep wave of frequency f_c (fig. 1(b)) determines the sampling intervals T_c. The two waveforms are combined in a summing circuit and are then compared with a reference or a control voltage in an absolute level comparator circuit as shown in figure 1(c). The comparator is an on-off device and is in the on state when the input voltage is greater than the control voltage. The intersections of the summed voltage waveforms with the control voltage therefore determine the widths of the pulses in the pulse train. The output of the comparator is the constant amplitude PWM signal waveform shown in figure 1(d). This signal is am-

(a) Modulating wave of frequency f_m and period T_m.

(b) Sampling wave frequency f_c and period T_c.

(c) Summed waves.

(d) Pulse-width-modulated signal.

(e) Pulse-width-modulated output voltage at filter input.
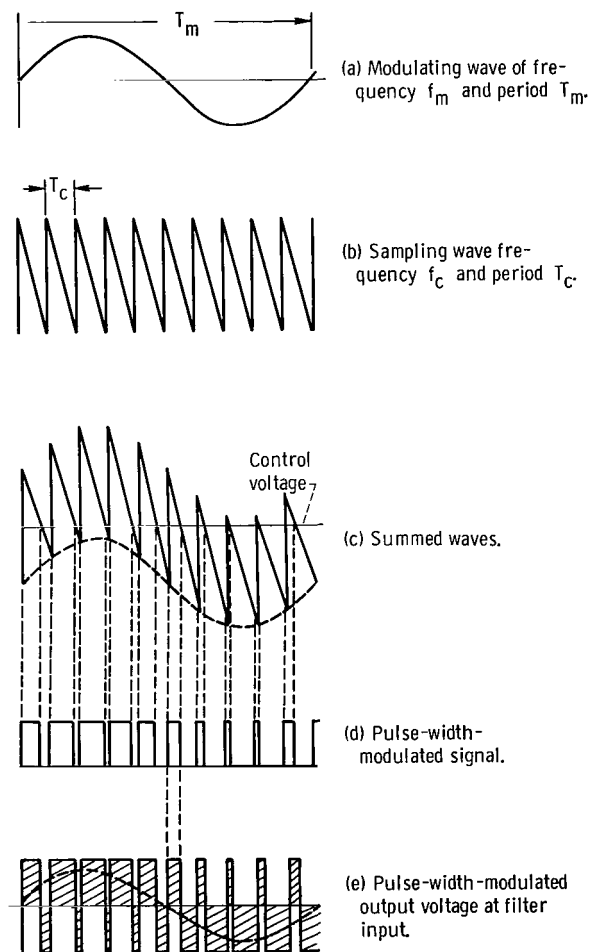
Figure 1. - Pulse width modulation.

plified further to drive a push-pull switching output power amplifier. The output voltage of the power amplifier is shown in figure 1(e), and the sine wave voltage is illustrated by the dotted sine waveform. This sine wave voltage is obtained by filtering the PWM voltage.

An important characteristic of a PWM wave is the modulation index. This index describes the degree of modulation of the PWM waveform and is defined by
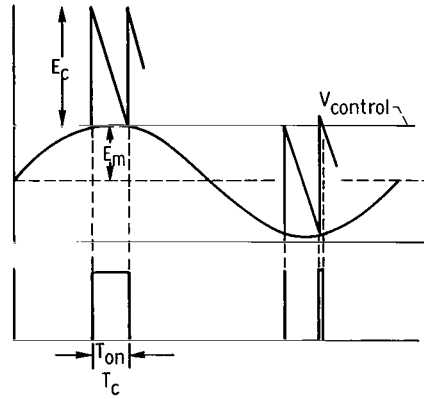
$$M = \left| \frac{T_{on} - \frac{T_c}{2}}{T_c/2} \right| \tag{1}$$

where M is the modulation index, T_c the time width of the sampling interval in seconds, and T_{on} the time width in seconds of the widest pulse in the pulse train. The conditions for modulation indexes of 0, 1.0, and 0.5 are illustrated in figure 2. In figure 2(a) the modulation voltage is zero and the intersections of the sweep wave with the control voltage produce a periodic pulse width $T_{on} = T_c/2$ and, from equation (1), a zero modulation index. This PWM signal results in a symmetrical square wave voltage of frequency f_c at the output filter and a zero output voltage after the filter.

A modulation index of approximately 1.0 is illustrated in figure 2(b). The peak voltage of the sweep wave E_c is equal to the peak-to-peak voltage of the modulating voltage $|E_m|$, and the maximum pulse width T_{on} is approximately equal to T_c. A high modulation index approaching 1.0 is desirable from high efficiency and high output voltage considerations for static inverters. But from equation (1) this requires an extremely narrow pulse of an infinitesimal time width at the negative peak of the modulating wave as illustrated in figure 1(b). This narrow pulse is not practically attainable because of the limitations imposed by the switching characteristics of the high power semiconductors used in the output power stages. The finite switching time of even high speed switching semiconductors limits the modulation index to a value less than 1.0. As an example, the narrowest pulse an exceptional power transistor with turnon and turnoff switching times of 1 microsecond can reproduce is approximately 5 microseconds. And this gives a modulation index of 0.9 at a sweep frequency of 10 kilohertz where $T_c = 100$ microseconds.

A modulation index of 0.5 is illustrated in figure 1(c). For this condition $|E'_m| = |E_m/2| = E_c/4$ and $T_{on} = 0.75 \, T_c$. The relations illustrated in figure 2 imply that both the modulation index and the sine wave output voltage $E_o \sin w_m t$ are linear functions of the amplitude of the modulation voltage $|E_m|$, when E_c and V control are constant.

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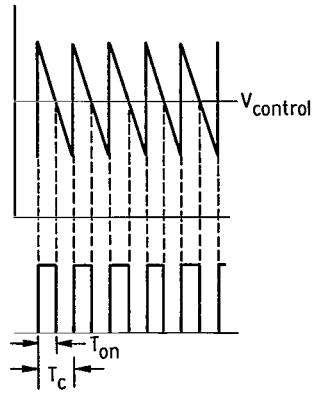
(a) M = 0; $T_{on} = T_c/2$; and modulation voltage = 0.

(b) M ≅ 1.0; $T_{on} \cong T_c$; modulation voltage = $|E_m|$ sin $w_m t$; and $|E_c/2| = |E_m|$.
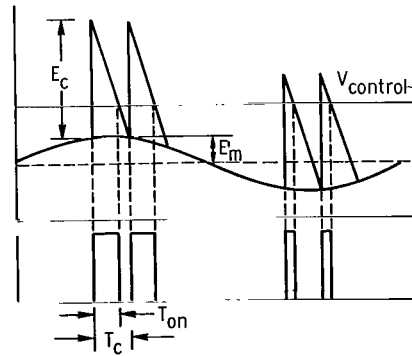
(c) M = 0.50; T_{on} = 0.75 T_c; modulation voltage = $|E_m'|$ sin $w_m t$; and $|E_c/4| = |E_m'|$.

Figure 2. - Conditions illustrating 0, 1.0, and 0.5 indices of modulation, $M\left[M = \left|\frac{T_{on} - T_c/2}{T_c/2}\right|\right]$.

PULSE-WIDTH-MODULATED DIRECT-CURRENT TO THREE-PHASE

ALTERNATING-CURRENT STATIC INVERTER

The basic circuits required for the experimental model of the PWM dc to three-phase ac static inverter are shown in block diagram form in figure 3. The complete inverter circuit consists of three separate but identical single-phase channels coupled through the 400-hertz, three-phase square wave signal generator circuit and the dc power supply and regulation loop. Each channel comprises one phase of the three-phase inverter and the three-phase square wave generator provides the 120° separation between phases. The 400-hertz sine wave modulating signals are derived from the square wave signals in the 400-hertz filter, and they are then combined in the summing amplifier with the 7.2-kilohertz sawtooth waveform voltages from the sawtooth generator. The slicer is a differential amplifier level comparator that compares the summed waveforms with a control voltage to produce the PWM signals.
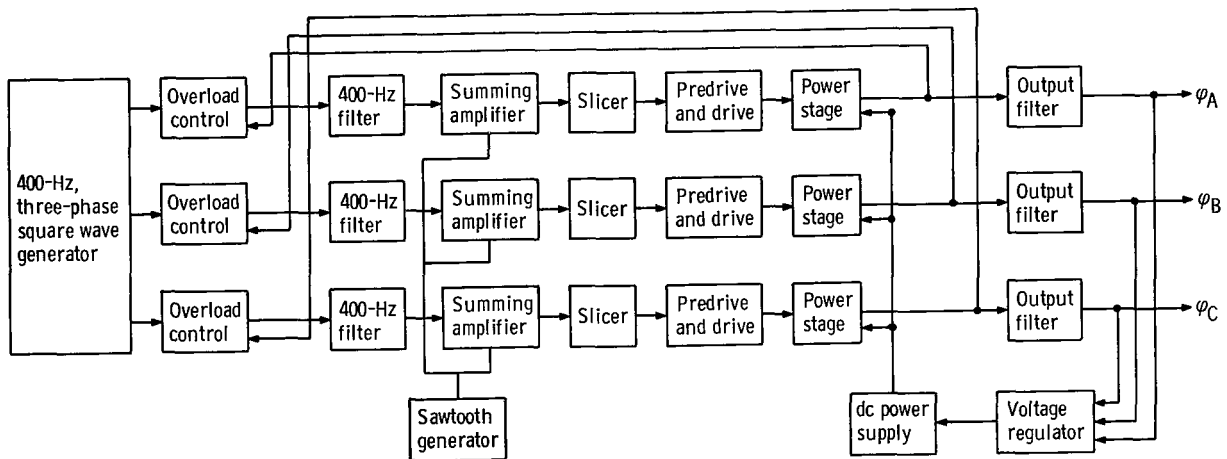
Figure 3. - Block diagram of pulse-width-modulated (PWM) inverter.

The PWM signals are amplified in the predrive circuit, and the drive circuit controls the switching of the power transistors in the power stage. The power stage is a half-bridge circuit with three parallel connected power transistors in each leg. Parallel transistors were required in this model because transistors with adequate voltage and current ratings for the power rating of this inverter were unavailable. A total of 18 power transistors are required for the three-phase power stages, and balancing reactors force equal current sharing among the three paralleled transistors. The output filter is an inductive capacitive (L-C) circuit with an air core inductor. This circuit

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filters the PWM voltage from the power stage to provide the 400-hertz sine wave output voltage.

Feedback loops are provided for overload current control and for output voltage regulation. The overload control is a variable attenuator circuit which reduces the modulation voltage and therefore the ac output voltage to limit the output current to a safe level. Output voltage regulation is accomplished by sensing the average output voltage of the three phases and controlling the dc input voltage to each power stage. The regulator circuit can be of the buck-boost or series type for inverter applications where the peak ac output voltage is less than the dc power supply voltage. But for applications where the ac output voltage is greater than the dc power supply voltage, a separate regulated dc-to-dc converter must be used to raise the dc voltage level because the output stage of the PWM inverter is transformerless. The output voltage could be regulated by varying the modulation index, but a high index increases the efficiency, so varying the dc supply voltage is generally preferred.

The experimental inverter described in this report requires a separate dc-to-dc converter because it was designed to operate from a dc supply voltage of 56 volts and produce a 400-hertz, three-phase output voltage of 120/208 volts. This report, however, describes the open-loop performance because the required dc high voltage to the power stages was obtained from a conventional laboratory dc power supply and the feedback loop for voltage regulation was inoperative. The design details and performance of the circuits identified in the block diagram for the experimental inverter model are discussed in the following sections.

CIRCUIT DESCRIPTION

Three-Phase Square-Wave Generator

The frequency and three-phase relations of the output are determined by the outputs of the three-phase square wave generator. The operation of the basic subcircuits in the generator is described in reference 5. A temperature-stabilized astable multivibrator generates a 2.4-kilohertz square wave. This square wave is used as a trigger pulse for three flip-flop circuits connected as a divide by a six ring counter. The output of each flip-flop is a 400-hertz square wave, and these three outputs are 120° out of phase with each other. A three input gate connected to the three flip-flop outputs checks and corrects the phase sequence. If the three outputs are not correct, then there is a time when all three outputs are high. The gate resets one of the flip-flops to zero whenever this occurs. Figure 4 shows the relations of the 2.4-kilohertz timing pulses and the 400-hertz outputs. (See figs. 21 to 23 for schematic diagrams of the circuits.)
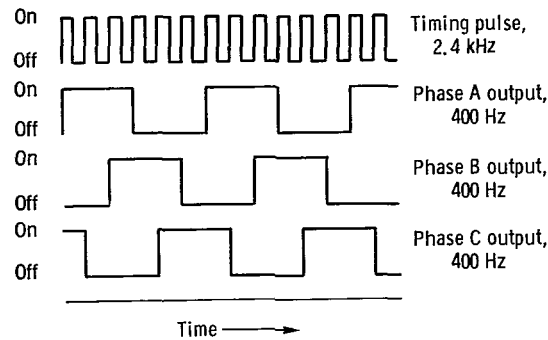
Figure 4. - Pulse relations of 400-hertz generator.

Overload Control

A current sensing circuit is connected to the inverter output to protect the power stage transistors from excessive collector currents in case of overload or short circuited output. The output current is limited by lowering the output voltage, which reduces the current proportionally. Each phase is protected independently, and each maintains a low distortion 400-hertz sine wave while overloaded.

The output voltage is reduced by lowering the modulation index. Figure 5 shows
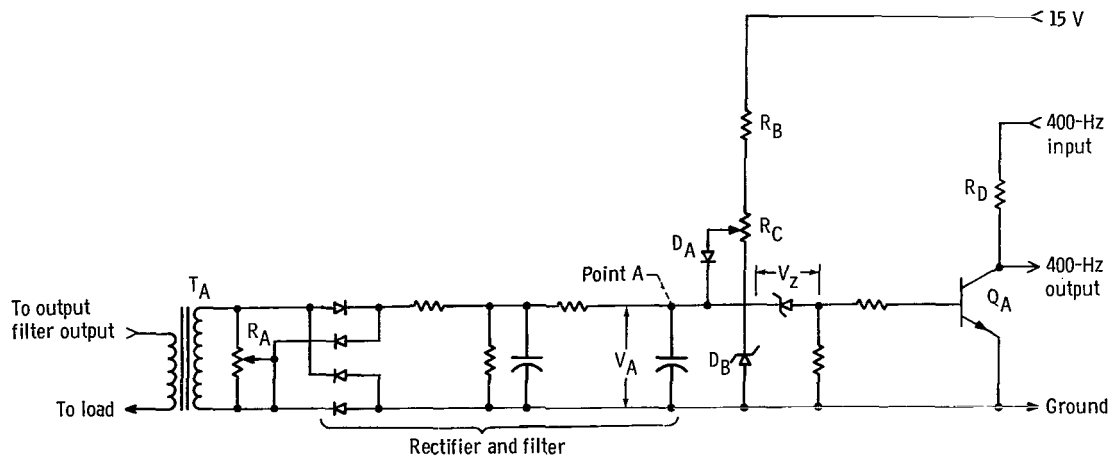
Figure 5. - Overload control for one phase.

the output current is sensed by the current transformer T_A at the inverter output. The adjustable burden R_A sets the secondary volts per primary ampere ratio. The secondary voltage is rectified and filtered to produce a dc voltage V_A which is proportional to the output current. If this voltage exceeds the zener diode voltage V_Z

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and the base emitter voltage of Q_A, then Q_A conducts.

The 400-hertz square wave from the three-phase generator is applied at the input of the overload control. If Q_A is not conducting, the output voltage is very nearly equal to input voltage. If Q_A is conducting, the output voltage is reduced because of the voltage divider action of R_D and Q_A. Reducing the output voltage reduces the amplitude of the modulating wave and therefore the modulation index and output current.

The output is reduced only enough to limit the current, and it returns to the normal regulated value when the overload is removed. To increase the response time of the circuit, the network consisting of R_B, R_C, D_A, and D_B biases point A to a value slightly below where Q_A starts conducting.

400-hertz filter. - A 400-hertz sine wave is required to generate the PWM signal. It is obtained from the 400-hertz square wave by filtering out all the harmonics of the square wave except the fundamental. The filter used is an encapsulated subminiature telemetry filter. This is a passive unit with a 60-hertz bandpass and 40-decibel-per-octave attenuation. The 400-hertz sine wave out of the filter is distorted by less than 1 percent. Most of this distortion is caused by the nonlinear loading of the summing amplifier.

Sawtooth generator. - The sawtooth generator provides the waveform used in sampling the 400-hertz modulating signal. The frequency of this sawtooth determines the carrier frequency, and for accurate modulation, the sawtooth should have a linear voltage rise with respect to time and a rapid voltage drop at the end of the cycle. Distortions in the sawtooth waveform result in approximately equal amounts of low frequency distortion in the inverter output, before the output filter.

In the circuit (fig. 6), timing capacitor C_A is charged from a constant current
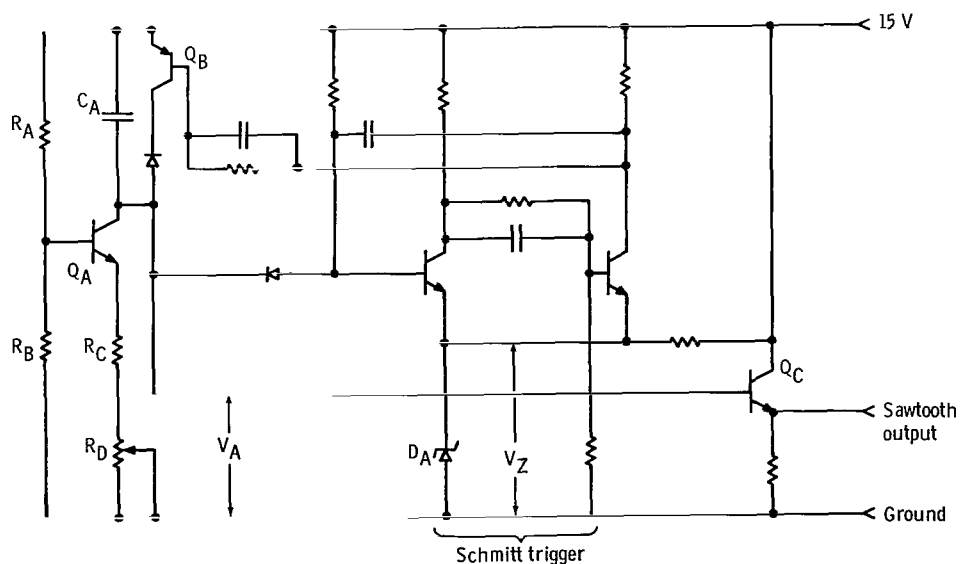
Figure 6. - Sawtooth generator.

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source consisting of Q_A, R_A, R_B, R_C, and R_D. Charging a capacitor with a constant current causes a linear voltage increase across the capacitor. When the voltage V_A decreases to V_Z, determined by D_A, the Schmitt trigger (ref. 5) switches, thus turning on Q_B. Capacitor C_A discharges through transistor Q_B, reducing its voltage rapidly and resetting the Schmitt trigger for the next cycle. Transistor Q_C is connected as an emitter-follower, whose emitter, the output, follows the capacitor voltage.

Summing amplifier. - The sawtooth carrier signal and the 400-hertz sine wave are combined in the summing amplifier. They are added linearly to produce the output shown in figure 7(a). Figure 7(b) shows one input applied to the base of Q_A and the other input to the base of Q_B. Because of the large emitter resistors, the transistor currents are proportional to the input voltages. The collectors are tied to a common collector load, so the voltage across this resistor is proportional to the sum of the
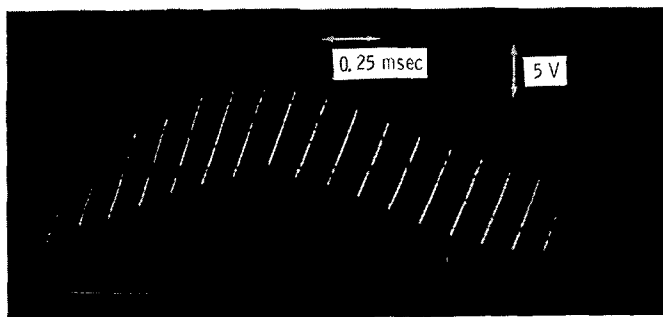
(a) Output.
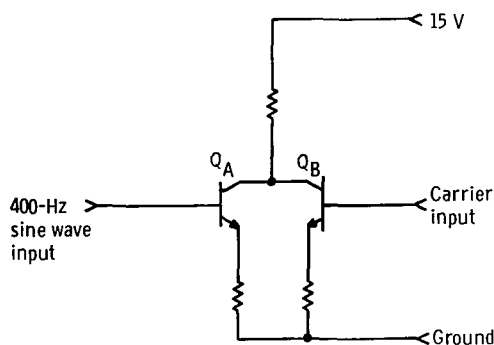
(b) Circuit diagram.

Figure 7. - Summing amplifier.

collector currents, and therefore the input signals.

Slicer amplifier. - The slicer amplifier is a high-gain differential amplifier and clipper, or voltage comparator. In this circuit (fig. 8(a)), the voltage V_A is compared to the reference voltage V_B, which is set by the variable resistor R_A. If V_A is greater than V_B, then Q_A conducts, Q_B turns off, Q_C turns off, and the output goes to zero. If V_A is less than V_B, then Q_A turns off and Q_B and Q_C are on, and

(a) Circuit diagram.

0.25 msec

5 V
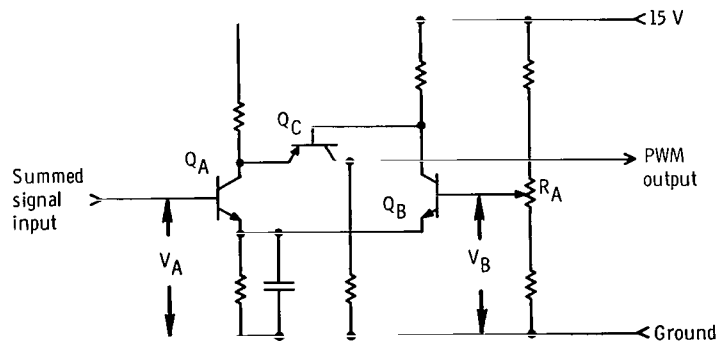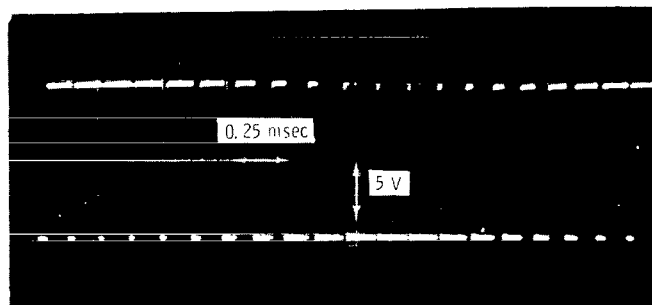
(b) Pulse-width-modulated (PWM) output.

Figure 8. - Slicer amplifier.

the output voltage is nearly 15 volts. The resistor R_A is adjusted to slice the input voltage symmetrically to provide a symmetrical PWM signal at the output. The modulation is completed at this point. Figure 8(b) shows the PWM signal produced.

Predrive. - The predrive circuit performs two functions:

(1) It amplifies the PWM signal.

(2) It generates turnon delay pulses which compensate for the noninstantaneous switching time characteristics of the power stage transistors (ref. 4). The circuit is shown in figure 9. The amplifier operates in a switching mode and supplies a push-pull signal to the two output transformers T_A and T_B. Transformer T_B is a linear transformer and therefore its secondary voltage is the PWM waveform. Transformer T_A is a saturable transformer and is designed to saturate after 10 microseconds. Its output therefore is a series of 10-microsecond pulses which occur each time the PWM signal switches. The pulse from T_A delays the turnon of the power stage transistors. Figure 10 shows the relation of the delay pulse to a typical section of the PWM wave.
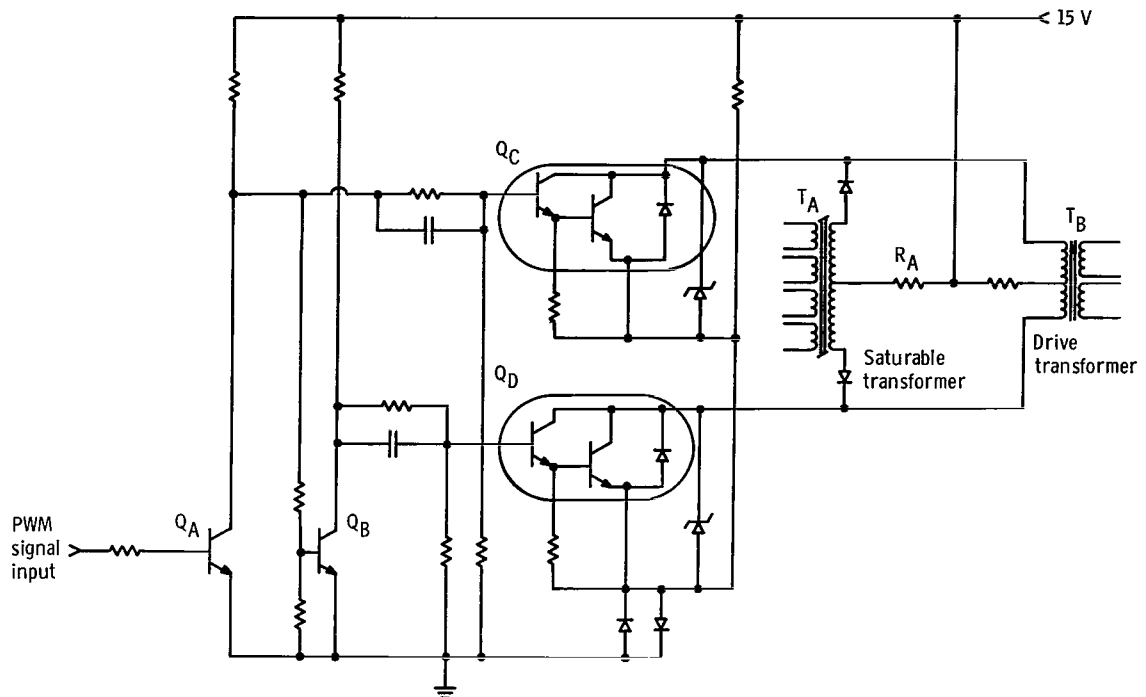
Figure 9. - Predrive circuit.
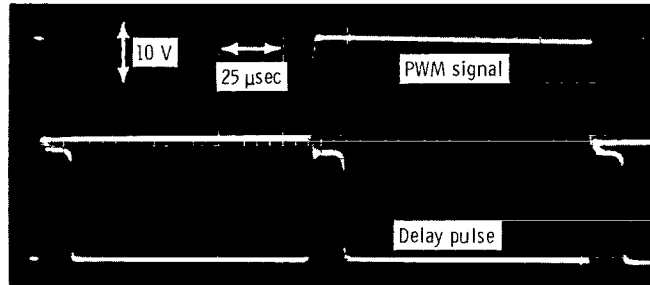
Figure 10. - Turnon delay pulse.

Drive circuit. - A common problem in bridge-type output stages is that the transistors in both the positive and negative halves (fig. 11) of the power bridge circuits conduct simultaneously during the switching interval, and thus they effectively short circuit the power supply while switching. The short-circuit current spikes that result reduce the efficiency, and, if they exceed the collector current ratings of the power transistors, cause catastrophic failures. The short-circuit conditions result from the finite switching characteristics of the power transistors (i. e., fall time and storage time delay during turnoff) and the response time of the drive circuits (ref. 4). The short-circuit currents can be limited by the use of protective reactors (ref. 6), but, in the inverter, the

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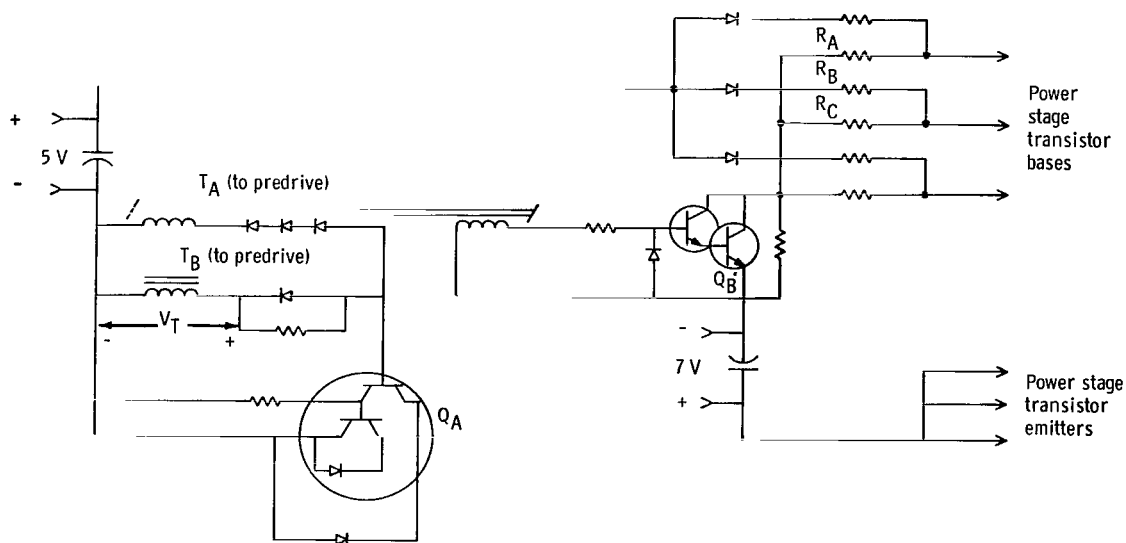
(a) One-half of one phase.
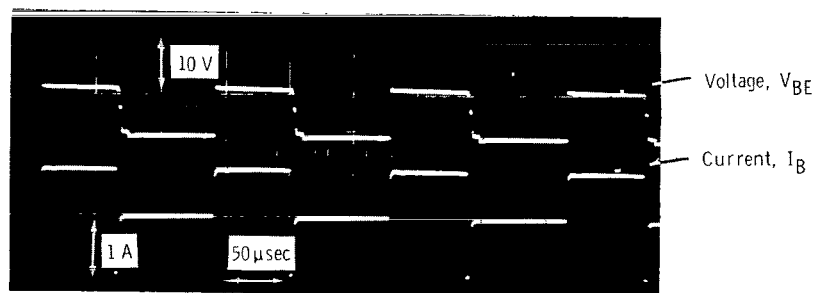
(b) Base drive waveforms.

Figure 11. - Drive circuit.

delay pulse generated in the predrive circuit is used to delay the turnon of one side of the bridge until the other side is turned off. The drive circuit and the resulting base drive waveforms are shown in figures 11(a) and (b).

The drive circuit used produces faster switching base drive waveforms than conventional transformer coupling and inserts a 10-microsecond delay to allow the opposite side of the bridge to switch off before beginning turnon. Also, a negative current is supplied to the base to decrease the turnoff time and storage delay. This reverse current is adjustable to equalize the turnoff times of the paralleled transistors; otherwise, the slowest transistor would carry excessive peak currents.

As shown in figure 11(a), drive power is provided by the 5-volt supply. Transistor Q_A is controlled by transformers T_A and T_B, and it switches base drive current to the paralleled power transistors. Whenever V_T is positive Q_A is turned on, except
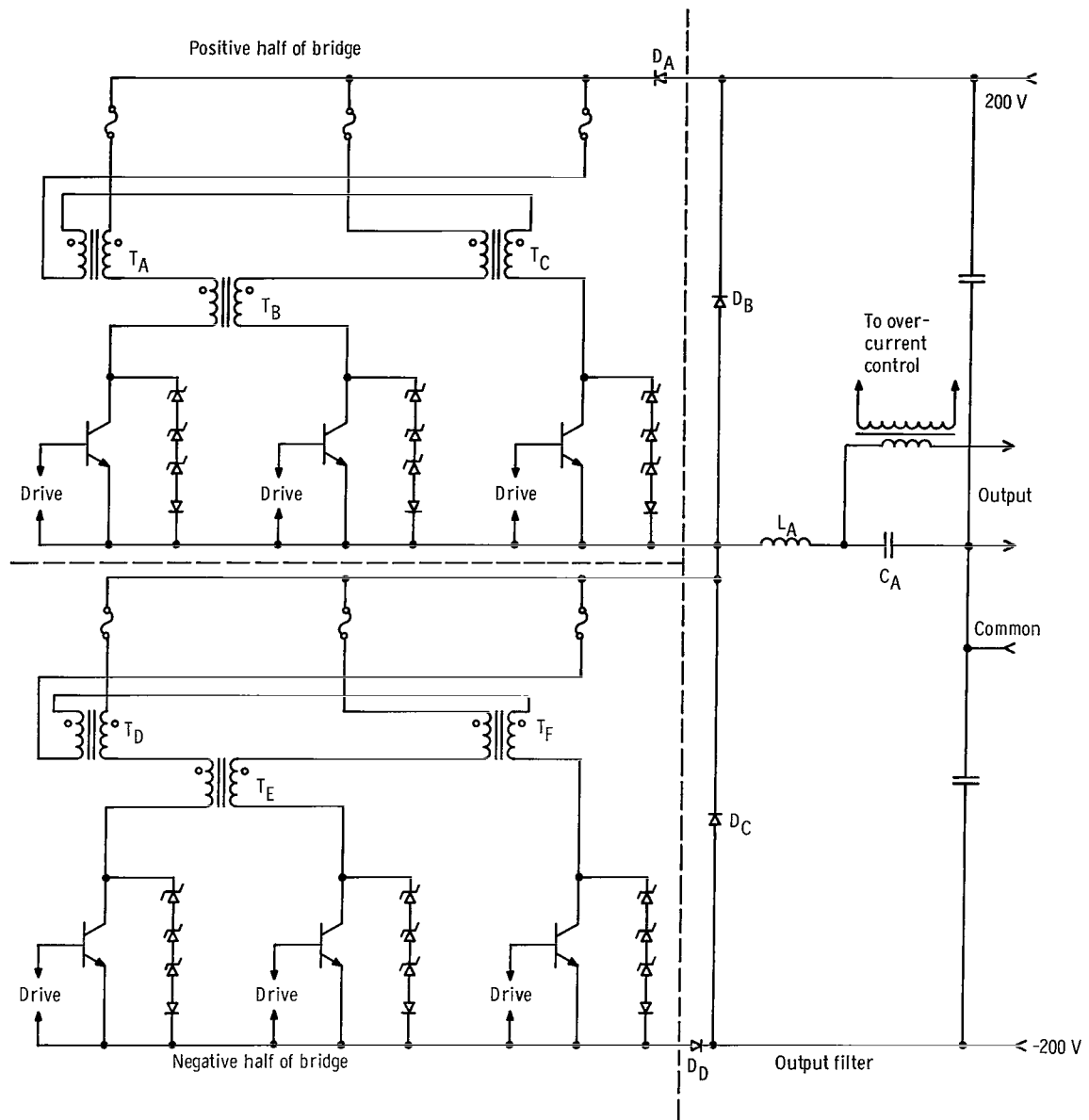
Figure 12. – Power stage of one phase.

at the start of each positive pulse when T_A produces a delay pulse. The delay pulse also turns on Q_B which connects the 7-volt supply to the transistor bases through the current limiting resistors R_A, R_B, and R_C. Adjusting these resistors balances the turnoff times by unbalancing the base currents.

Power stage and output filter. - The inverter output stage consists of three half-bridge circuits (one for each phase), each containing three paralleled transistors per leg, in order to provide sufficient current carrying capability. All phases are fed from one center-tapped power supply, but each bridge output is connected to a separate

single section L-C filter. Protective diodes and balancing reactors are also included. The complete diagram of one phase is shown in figure 12.

Diodes D_B and D_C return the reactive currents from the load and output filter to the supply, while D_A and D_D prevent reverse currents from flowing through the bridge. The balancing transformers T_A through T_F force equal current sharing in the paralleled transistors. At turnoff, these transformers are not effective, but the drive circuit can be adjusted to equalize the turnoff times and therefore the currents during turnoff. The zener diodes across each transistor clip the voltage spikes at turn-off to a safe level for the transistors.

The output filter consists of an air core inductor L_A and a capacitor C_A in a simple L-section filter. It provides a 6-decibel-per-octave attenuation, giving a 15-decibel attenuation at the carrier frequency. Figures 13(a) and (b) indicate typical collector currents and inverter output voltage waveforms.
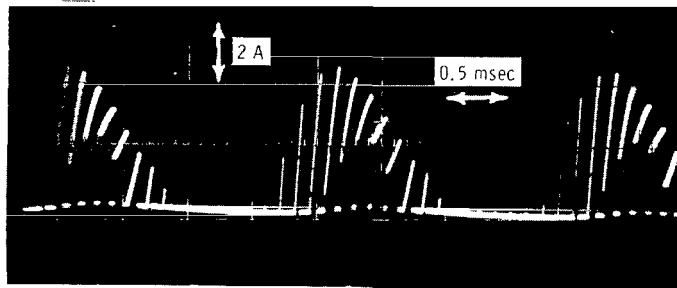
(a) Collector current of power transistor.
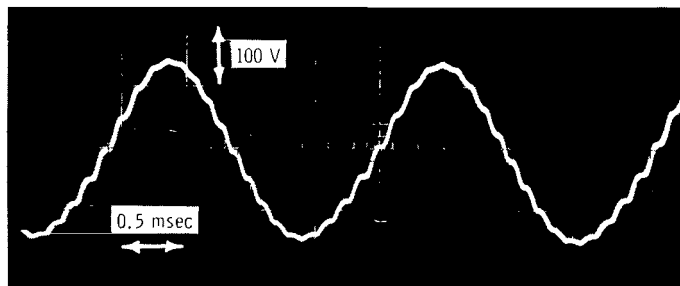
(b) Output voltage.

Figure 13. - Power transistor collector current and output voltage waveforms for PWM converter.

Experimental breadboard. - A breadboard to evaluate the performance was built using natural convection heatsinks and hand wiring throughout. Figure 14 shows the general layout and locations of sections shown in the block diagram (see fig. 3). The large heatsinks used for the power stage each mounted a pair of power bridge transis-

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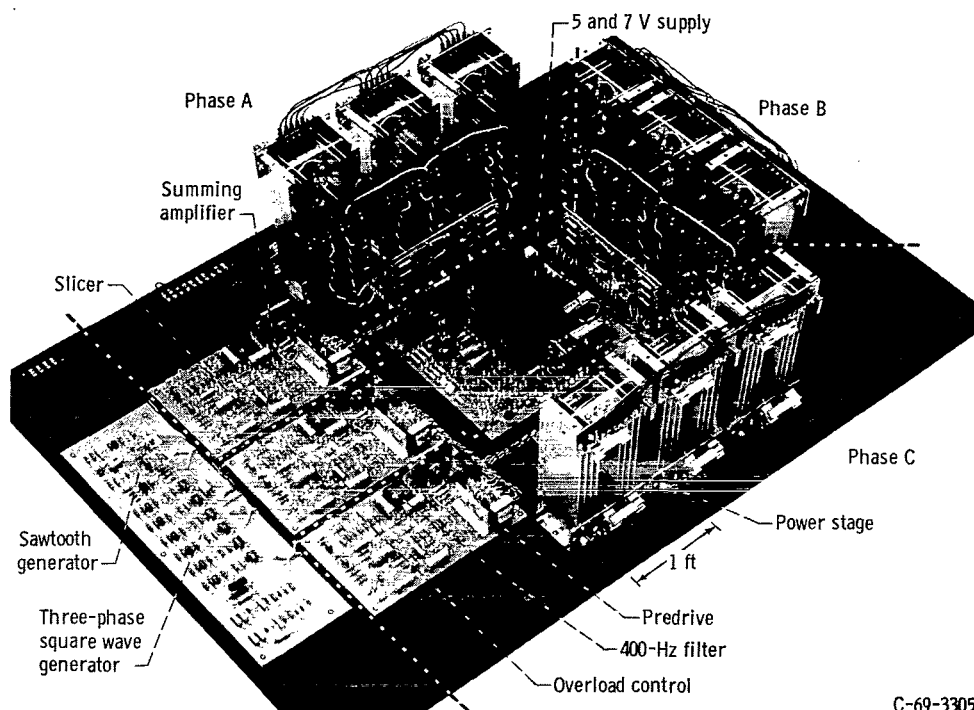
Figure 14. - Breadboard construction.

tors and their associated zener protection. The control circuits through the predrive stage occupy the four vectorboards on the left side of the breadboard. Discrete components were used because integrated circuits were not readily available when the circuit was designed. Use of integrated circuit and printed circuit boards could reduce the size by a factor of four quite easily. The vectorboard with the heatsink in the center of the breadboard is a dc-to-dc converter which supplies 5 and 7 volts for the drive circuits.

TEST PROCEDURES AND APPARATUS

The circuit used to test the inverter is shown in figure 15. Power was obtained from commercial power supplies. The 15 volts required for the control circuits (zener regulated separately for isolation) was obtained from the 56-volt supply. The 36-volt supply powered an internal dc-to-dc converter supplying 5 and 7 volts for the drive circuits. The inverter output was measured with 1/4-percent wattmeters and true rms voltmeters. The output current measurements, used only to set the load power factor, were made with panel meters. Power bridge input voltage was read digitally. Input current measurements used 1/4-percent millivoltmeters and dc shunts. Clamp-on
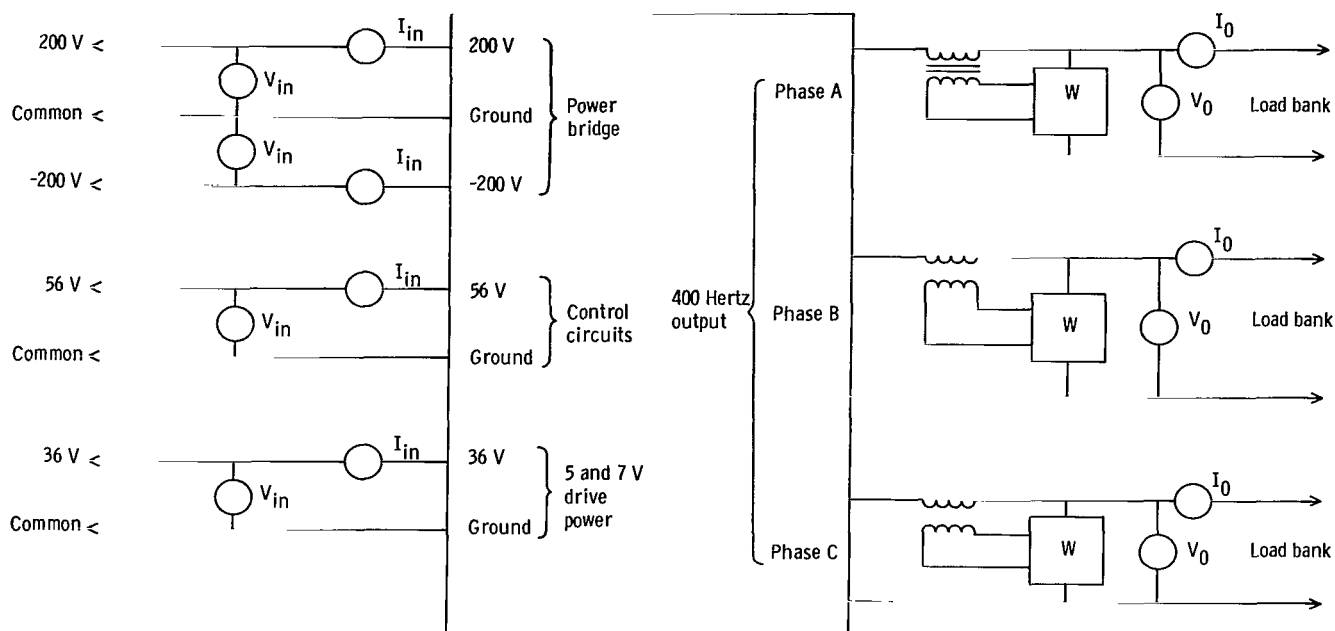
Figure 15. - Test setup.

current probes were used for oscilloscope pictures and power consumption measurements in the control sections. A wave analyzer was used for the harmonic analysis.

Except where stated, all tests were run at a 112-volt ac output, with the index of modulation set near 91 percent. Single-phase operation was used to simplify the testing, but the unit was run as a three-phase system successfully.

RESULTS AND DISCUSSION

One of the advantages of PWM inverters over other switching inverters is the reduction in output filter size. Total harmonic distortion at the bridge output (before the filter), computed by finding the rms value from the harmonic components listed in table I, is 120 percent, and the first component which exceeds 2 percent of the 400-hertz output (fundamental frequency) occurs at 5600 hertz. The second and third harmonics before the filter are only 2.0 and 0.4 percent of the fundamental, respectively, and are largely due to circuit nonlinearity. The carrier frequency (see table II), which is 18 times the fundamental 400-hertz output frequency, produces the largest single distortion component, 67 percent. Figure 16 shows the spectrum at the output of the output filter which consists of a 1-millihenry inductor and 12-microfarad capacitor. The carrier component was reduced to less than 2 percent by the filter. Although large heavy air-core inductors were used, the total filter weight can be less than $2\frac{1}{2}$ pounds per kilowatt. The total distortion of the 400-hertz sine wave output waveform is 6.5 percent, calculated as before from tables I and II or figure 16.

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TABLE I. - MAJOR COMPONENTS OF OUTPUT VOLTAGE[a]

Frequency, Hz	Harmonic percentage		Frequency, Hz	Harmonic percentage	
	Before filter	After filter		Before filter	After filter
400	100	100	7 600	33	0.8
800	2	3	8 000	33	.7
1200	.4	5	8 400	17	.3
1600	.4	.5	8 800	6	.1
2000	.4	.2	9 200	2	.03
2400	.2	.1	12 000	5.4	.05
2800	.15	.03	12 400	10.5	.1
3200	.25	----	12 800	15	.13
4400	.3	----	13 200	12	.1
4800	.6	.03	14 000	13	.09
5200	1.7	.1	14 400	40	.25
5600	6	.25	14 800	12	.08
6000	17	.7	15 600	12.5	.07
6400	33	1.2	16 000	14	.05
6800	33	1.2	16 800	6	.03
7200	67	1.8	17 200	4	----

[a]Harmonics listed are 0.03 percent or more of inverter output voltage.

TABLE II. - CARRIER FREQUENCY

HARMONICS

Frequency, kHz	Harmonic percentage[a]	
	Before filtering	After filtering
7.2	67	1.8
14.4	40	.25
21.6	30	.09
28.8	22	----
36.0	16	----
43.2	12	----
50.4	9	----

[a]Harmonic percentages computed with respect to 400-Hz output frequency.
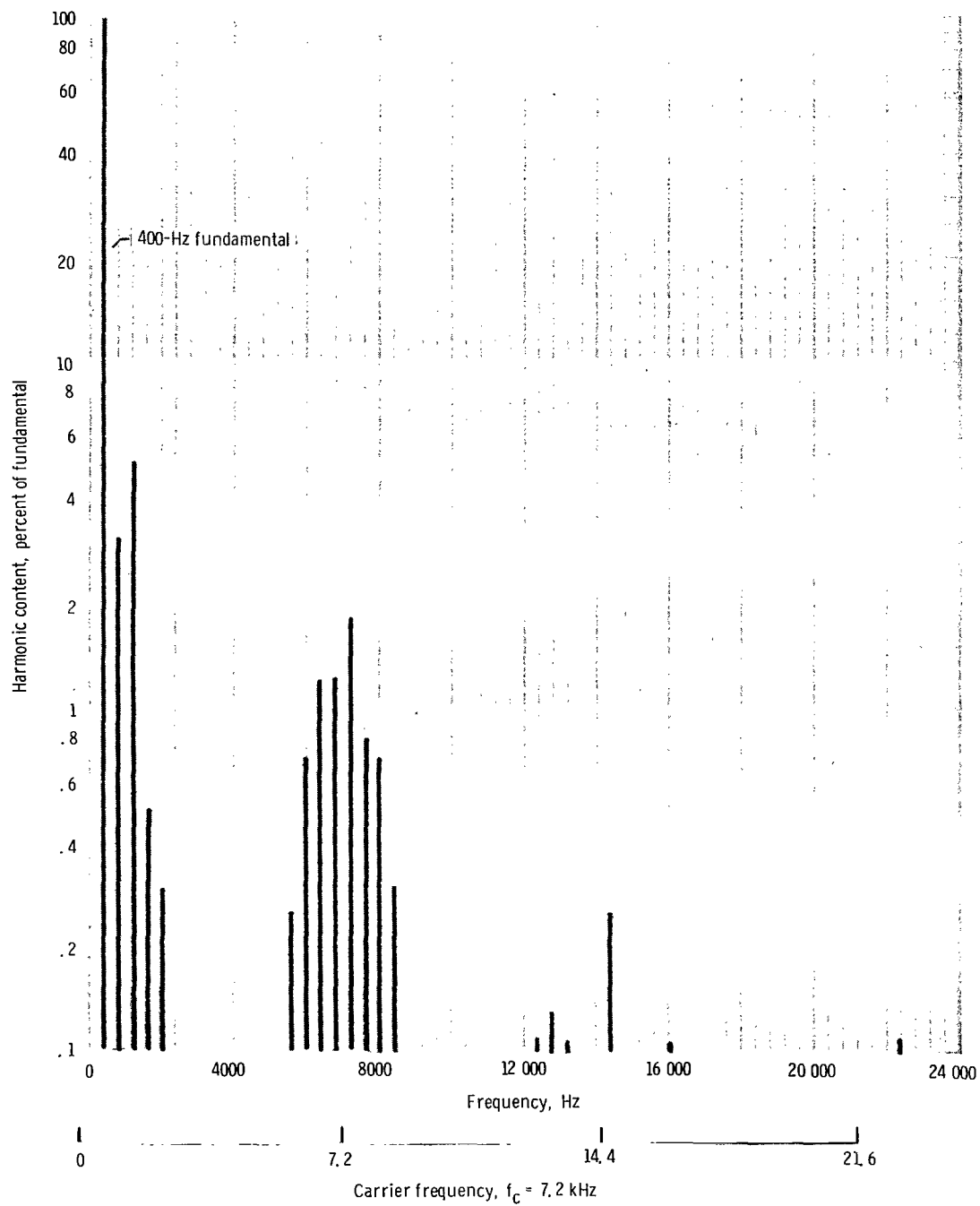
Figure 16. - Harmonic content of output voltage.

Voltage regulation in this inverter is obtained by varying the dc supply input voltage. Figure 17(a) shows the output voltage as a function of load for a constant input voltage. The voltage peaking evident at less than 200 volt-ampere loads with lagging power factors is caused by a resonance of the output filter capacitor with the load inductance. The dc power supply must be capable of producing 190 volts plus or minus approximately 10 percent for complete regulation. Figure 17(b) indicates the input voltage required as a function of load. Because of the limits of the power supplies used, the data were taken with the inverter operating at 112 volts ac and a maximum of 700 volt-amperes per phase. Since all three phases operate from one dc supply, they cannot be regulated independently. Therefore, with unbalanced loads, the output voltages are not balanced. If independent regulation is desired, either three separate supplies must be used, or the modulation indices should be varied, which would change the output voltages independently.

Power factor
□ 1.0
○ .7
△ .1

(a) Effect of load on output voltage for constant dc input voltage, E_{in}, 168 volts.

(b) Input voltage (E_{in}) required for constant ac output voltage, E_{out}, 112 volts (line to neutral).
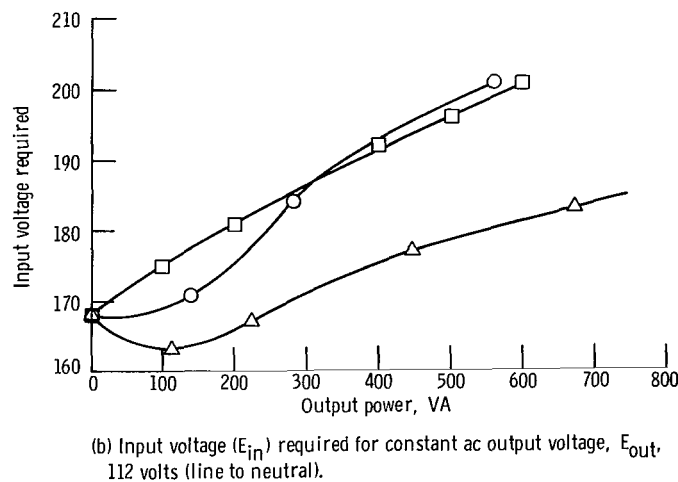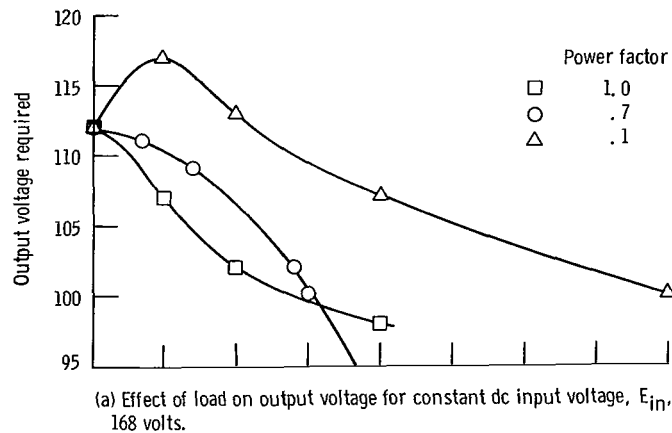
Figure 17. - Voltage regulation.

Power output stage. - This inverter used three transistors in parallel per leg, with
forced current sharing derived from the balancing transformers mentioned earlier.
Collector currents were balanced within 5 percent by use of these transformers, but the
switching speed adjustment, necessary to prevent excessive collector currents, was
difficult to adjust properly and required readjustment with component aging. The col-
lector emitter voltage was 410-volt peak PWM wave. A typical collector current wave-
form for a resistive load was shown in figure 13(a). A comparison with figure 18 re-
veals the negligible effect of a lagging power factor load.
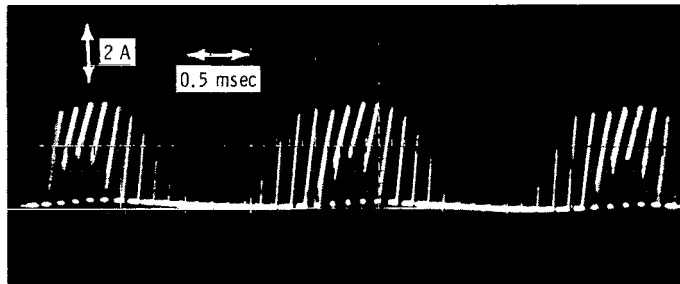
Figure 18. - Output transistor collector current with 0.7 power factor lagging
load.

The power stage with parallel transistors was found to be reasonably efficient as
is shown in figure 19. At the rated load of 2.5 kilovolt-amperes (582 W per phase at
0.7 power factor), the efficiency was 77.5 percent. Figure 19 shows that the maximum
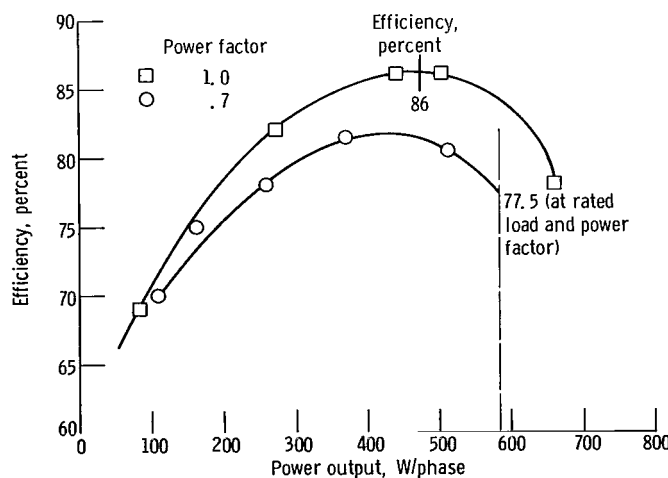
Figure 19. - Power stage efficiency as function of power output. Out-
put voltage (ac) E_{out}, 112 volts; frequency, 400 hertz.

efficiency for unity power factor load is 86 percent, and this occurs from 425 to 500 watts per phase. These tests were run at 112 volts ac output; a higher output voltage would have resulted in a higher efficiency.

Losses could be reduced considerably with faster transistors and larger more efficient output filter inductors. The efficiency shown is for the power output stage and filter only and excludes the drive and control circuit losses. These losses are presented in a later section.

Each phase was tested at 112 volts ac output, and a maximum of 700 volt-amperes per phase because available power supplies could only supply 202 volts. With 210-volt supplies (the maximum which is limited by zener diodes around the power transistors), the 117-volt ac 2.5 kilovolt-ampere three-phase rating would be obtainable according to calculations. The maximum output current is limited by the collector current ratings or the inverter's internal impedance which reduces the output voltage with large loads.

Because the output stage is directly coupled to the load, there is a possibility of a dc component in the output due to modulator unbalance. The dc component could be controlled to a low level (less than 1 V) quite easily with the balance adjustment, or could be eliminated by adding an isolation capacitor at the inverter output.

Employing a series connection of high current transistors in the bridge could eliminate the need for paralleling because higher current transistors are available at the lower voltage rating. The most common series arrangement is the full-bridge circuit using four transistors. The voltage requirements are then halved, allowing the use of faster, higher gain, and higher current transistors. The disadvantages are a more complex drive circuit and a separate isolated dc supply for each phase.

Drive circuit analysis. - Output transistor switching speed, a function of the base drive current, is an important factor in the power stage efficiency. The drive circuit used in this inverter increased the efficiency approximately 4 percent over a simple transformer coupled base drive (ref. 4). Drive circuit power consumption increases slightly though, and the circuit is more complex. Besides the added components in the drive circuit, a small converter was required in this inverter to supply the drive and turnoff power.

Drive current was 1.35 amperes at 5 volts for each leg of the bridge. Drive power could have been obtained more efficiently from a proportional feedback current transformer connected in the output stage. Drive current would then be proportional to the load current, thereby increasing the efficiency at low output power.

The transistor turnoff circuitry required only 2 watts per phase and reduced the turnoff time to one-fifth the time measured with transformer coupling. Also, turnoff times of several different transistors can be equalized by adjusting a single resistor for each transistor.

Control circuit. - When the inverter was designed, integrated circuits were not readily available. Therefore, although the inverter operates acceptably, the power consumption (34 W) and the size (see fig. 14) of the control section are somewhat larger than desired. The use of integrated circuits would reduce the size and power drain and generally increase the reliability. Figure 20 illustrates one possible system where integrated circuits are used to replace various blocks in the discrete system.
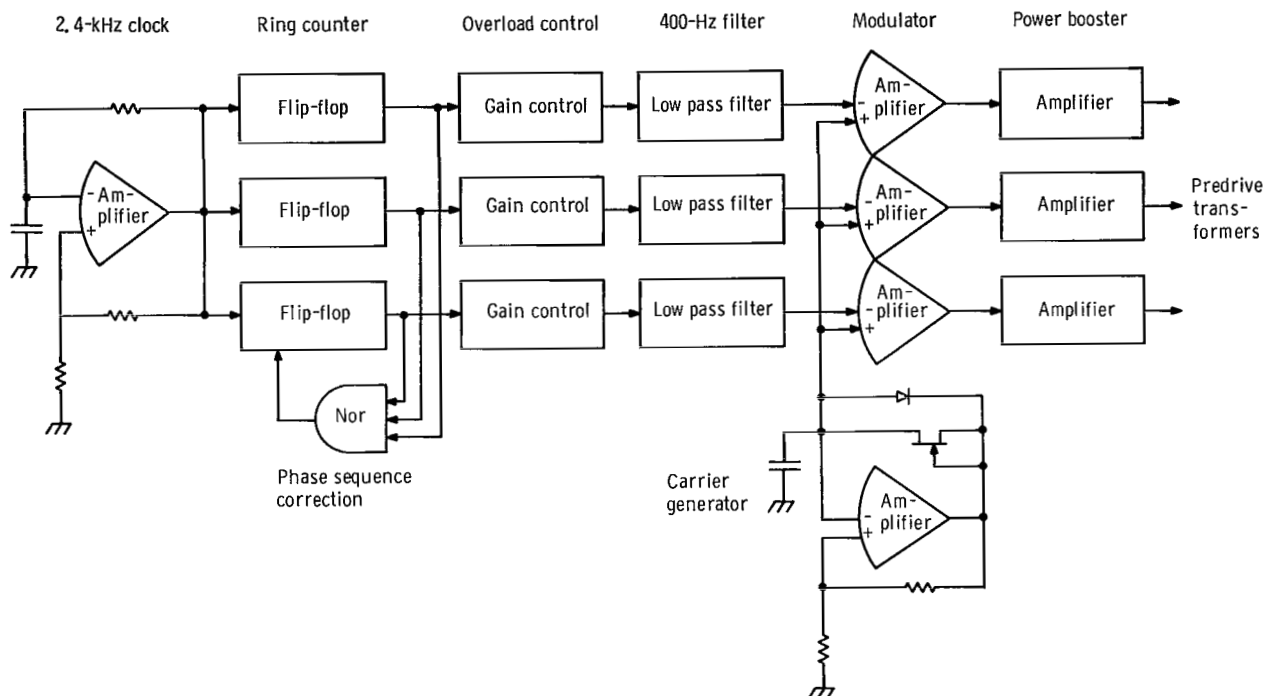

Figure 20. - Integrated circuit logic system.

An operational amplifier is connected as a multivibrator to generate the 2.4-kilohertz square wave. The square wave is divided by a ring counter as before, only this time the entire ring counter and phase sequence gate require just three parts. The original overload controls and 400-hertz filters can be used, although integrated circuit automatic gain control circuits and active filters may also be usable. Another operational amplifier is connected in a multivibrator connection to generate the sawtooth carrier, and only one operational amplifier per phase performs the slicing and clipping functions. A hybrid booster would then take the place of the predrive amplifier, and the only added complication would be the need for ±15-volt supplies. An added advantage is that the inherent matching of monolithic devices would eliminate some of the balance adjustments.

CONCLUDING REMARKS

A three-phase 2.5 kilovolt-ampere breadboard inverter was built to investigate the operation of a pulse-width-modulated (PWM) inverter. The test results and circuitry provided the basis for this report.

Since the carrier frequency of the PWM inverter is much higher than the output power frequency, only a small low loss output filter is required for a sinusoidal wave shape. Tests herein showed approximately $6\frac{1}{2}$ percent total harmonic distortion, but this could easily be reduced with a minimal increase of filter size.

Harmonics of the 400-hertz output power frequency can result from nonlinearities of the PWM circuits and unbalances of power transistor switching. It is important to minimize these effects since the small high frequency output filter does not attenuate low frequency harmonics.

The peak measured efficiency of the output stage is 86 percent at a unity power factor load. The efficiency at rated output is 77.5 percent, and it can be increased with further circuit improvements and optimization.

Careful balancing the PWM circuits is necessary to prevent a dc component of current flowing in the ac power output. Integrated circuits can assist in reducing the unbalance.

Regulation of the inverter ac output voltage can be achieved by controlling either the modulation index or the dc input voltage. But control of the dc voltage results in a higher efficiency. Control requirements for a 0.7 lagging power factor load for this inverter are ±10 percent of a nominal dc voltage of 190 volts. Closer output regulation tolerances for unbalanced loads can be obtained with separate dc voltage regulators for each phase.

The advantages of the half-bridge power circuit are that it requires fewer transistors and provides a three-phase four-wire output from a single dc supply. A limitation is that it requires high voltage transistors, which may not readily be available with high current ratings.

A full-bridge circuit requires more transistors but the required voltage rating is only half of the rating required for the half-bridge circuit. This is an advantage with regard to transistor availability and tradeoffs among voltage, current, and switching speed characteristics.

The delayed turnon and fast turnoff circuits for the power transistors minimized short-circuit current surges and provided fast switching with lower power loss.

Standard digital and linear integrated circuits reduce the size, power consumption,

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and complexity of the low level circuits. They also reduce the balancing problems of these circuits.

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        Cleveland, Ohio,
            120-27.

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Figure 21. - Logic for each
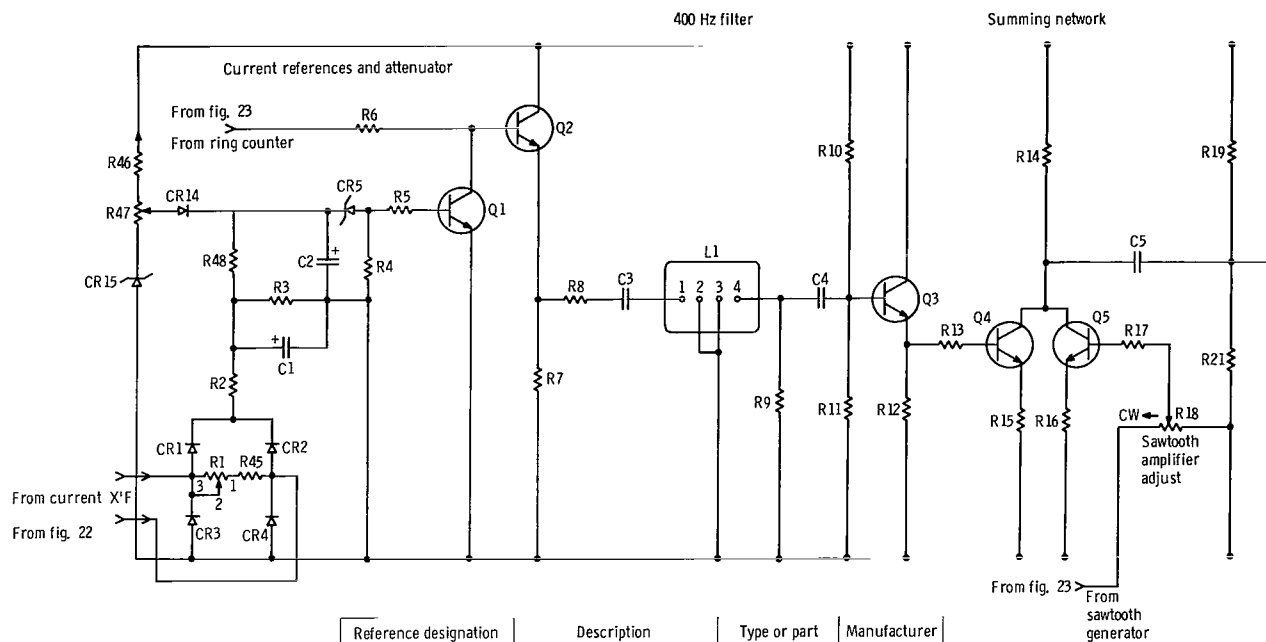
Reference designation	Description	Type or part number	Manufacturer
°C1	6. 8 µF, 20 V, 20%	150D685X0020B2	Sprague
°C2	580 µF, 15 V, 20%	112D587C7015P1	Sprague
C3 to C5, C7	0. 33 µF, 150 V, 10%	617G33491, 5W2	Good-All
C6	0. 1 µF, 150 V, 10%	671G10491, 5W2	Good-All
C8, C9	0. 0012 µF, 55 V	DM-19-122J	Arco-Elmenco
°C10, C11	100 µF, 20 V, 20%	150D107X002052	Sprague
CR1 to CR4, CR14	Silicon diode, 175 V, 500 mW	1N485B	Fairchild
CR5	Zener diode, 5. 1 V, 400 mW, 5%	1N751A	Motorola
°CR6, CR7, CR10, CR11	Silicon diode, 3 A, 200 V	UTR-3320	Unitrode
°CR8, CR9	Zener diode, 39 V, 1 W, 5%	1N3034B	Motorola
CR12, CR13	Zener diode, 15 V, 10 W, 5%	1N2979B	Motorola
°Filter 1	400-Hz filter, band pass	MNF. 4	UTC
Q1 to Q7, Q9, Q10, Q11	Silicon transistor, 30 V, 800 mA	2N2222	Motorola
°Q8	Silicon transistor, 40 V, 600 mA	2N2904	Motorola
°Q12, Q13	Silicon transistor, 60 V, 7 A, Darlington	2N3230	RCA
R1	200 Ω pot, 1 W wire wound	3280W-1-201	Bourns
R2	68 Ω $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R3, R14, R25, R32	2700 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R4, R33, R37, R38	4700 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R5, R6, R19, R30	22 000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R7, R31, R34, R41	1000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R8, R12, R28	10 000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R9, R11	27 000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC

°Parts not on JPL Spec. ZPP-2061-PPL-F.

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Slicer Driver

15 V dc

R20 R23 R27 R28 R31 R34 C8 Q12 R41 CR10 T1 T2
Q7 Q8 Q9 R29 R32 Q11 R35 R37 R39 CR8 B R42 R43 To fig. 22
Q6 R33 CR6 CR6 CR7 B CR9
R22 R24 C6 R26 Q10 C9 R38 R40 To fig. 22 CR11
R25 C7 R30 R36 Q13 + C10 Ground
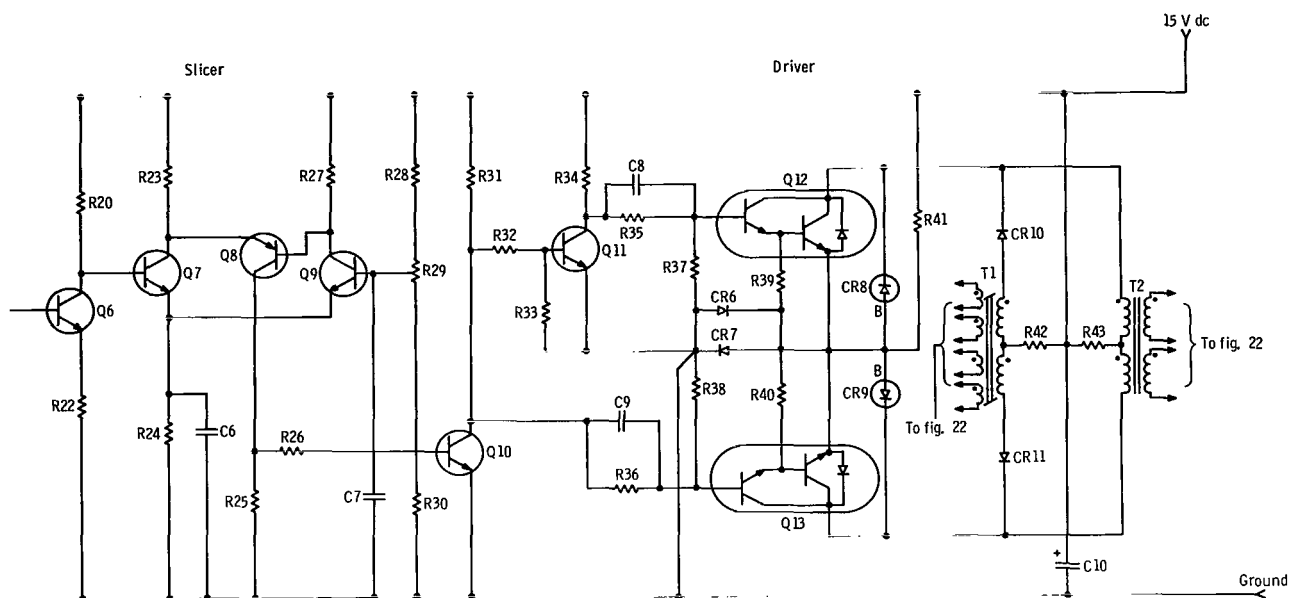
Reference designation	Description	Type or part number	Manufacturer
R10	68 000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R13, R17	47 000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R15, R16	3900 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R18	20 000 Ω pot, 1 W wire wound	3280W-1-203	Bourns
R20, R24	2200 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R21	6800 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R22	1200 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R23	2000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R26, R27	1500 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R29	10 000 Ω pot, 1 W wire wound	3280W-1-103	Bourns
R35, R36	680 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R39, R40	47 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
°R42	30 Ω, 25 W, 1%	MC-250	Cal-R
°R43	2.5 Ω, 5 W, 1%	NS-5	Dale
°R44	65 Ω, 50 W, 1%	RHM-50	Dale
R45	75 Ω, 5 W, 1%	5A-50	Cal-R
°T1	Saturable transformer	B305710	TRW
°T2	Drive transformer	B305711	TRW
R46	2200, 1 W, 5%	GBT-1	IRC
R47	300 Ω pot, 1 W	3280W-1-501	Bourns
R48	330 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R49	330 Ω, 10 W, 1%	RHM-10	Dale
R50	39 Ω, 1 W, 5%	GBT-1	IRC

°Parts not on JPL Spec. ZPP-2061-PPL-F.

phase of PWM static inverter.

27
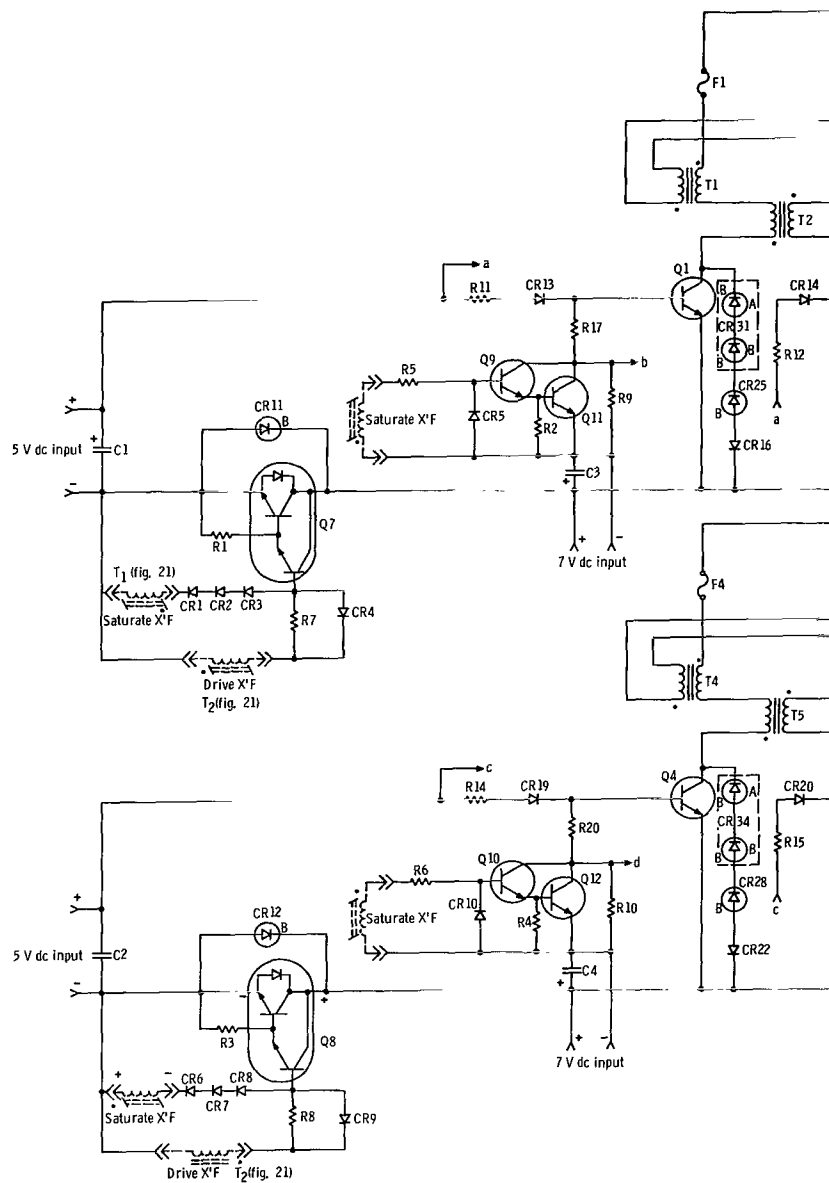
Reference designation	Description	Type or part number	Manufacturer
*C1 to C4	Three 100 μF, 20 V, 10% capacitors in parallel	150D10X902S2	Sprague
*C5, C6	125 μF, 200 V ac, 10% 60 μF, 200 V ac, 10%	333P14 333P13	Sprague Sprague
*C7	Four 4 μF, 300 V, 10% capacitors in parallel	260P40593T7	Sprague
CR1 to CR10	Diode, 100 V, 250 mW, fast recovery	1N916	Fairchild
CR11, CR12	Zener diode, 27 V, 1 W, 5%	1N3030B	Motorola
*CR13 to CR24	Diode, 3 A, 200 V, fast recovery	UTR-3320	Unitrode
CR25 to CR30	Zener diode, 10 V, 10 W, 5%	1N2974B	Motorola
*CR31 to CR36	Zener diode, 400 V, 100 W, 2% (two 200 V diodes in series)	50M200ZB2	Motorola
CR43, CR44	Diode, 12 A, 400 V, fast recovery	1N3888	Hughes

*Parts not on JPL Spec. ZPP-2061-PPL-F.

Figure 22. – Power stage schematic of one phase for a

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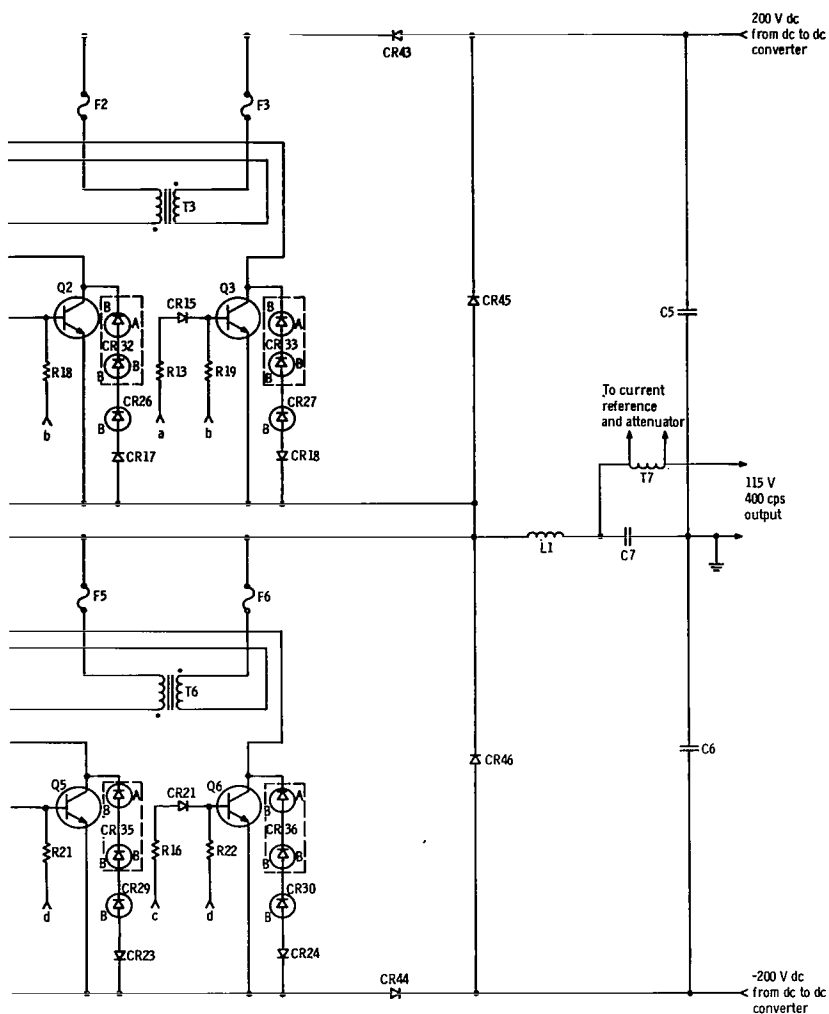
Reference designation	Description	Type of part number	Manufacturer
*CR45 to CR46	Diode, 12 A, 600 V, fast recovery	479M	Westinghouse
*F1 to F6	4 A fuse	A25X4	Chase–Shawmut
*L1	Filter inductor	305897	TRW
*Q1 to Q6	Transistor, 5 A, 500 V, selected $V_{ces(ses)}$ > 400 V	DTS-0710 (selected, 7299751)	Delco
*Q7, Q8	Transistor, 7 A, 60 V, Darlington	2N3230	RCA
*Q9, Q10	Transistor, 5 A, 60 V	2N2657	Minneapolis– Honeywell (Solitron)
*Q11, Q12	Transistor, 25 A, 60 V	2N3264	RCA
R1 to R4	47 Ω $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R5, R6	82 Ω $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R7, R8	100 Ω $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R9, R10	150 Ω 1 W, 5%	GBT-1	IRC
*R11 to R16	2 Ω, 5 W, 1%	NS-5	Dale
*R17 to R22	1 Ω, 5 W, 1%	NS-5	Dale
*T1 to T6	Balancing reactor	305896	TRW
*T7	Current transformer	305898	TRW

*Parts not on JPL Spec. ZPP-2061-PPL-F.

three-phase, 2.5 kilovolt-ampere PWM static inverter.
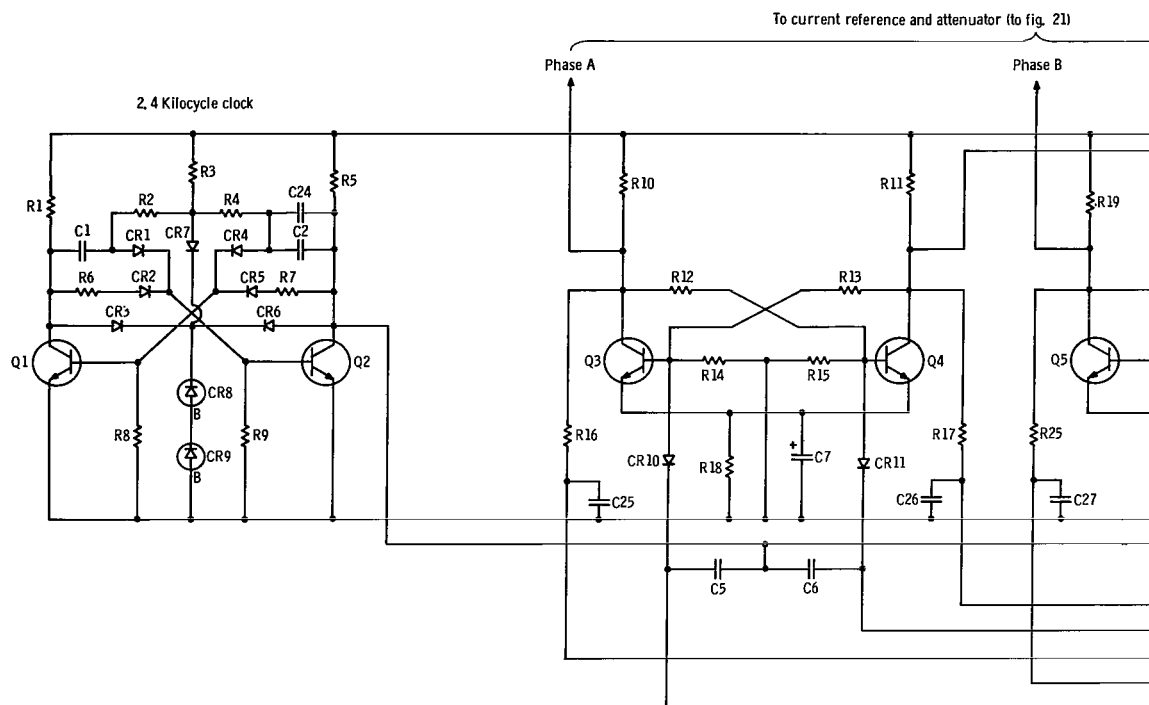
Reference designation	Description	Type or part number	Manufacturer
C1, C2	0.01 µF, 150 V, 5%	617G10351, 5W2	Good-All
C3, C4, C8, C9, C13, C14	470 µF, 300 V	DM-15-471J	Arco-Elmenco
C5, C6, C10, C11, C15, C16	0.0027 µF, 500 V	DM-19-272J	Arco-Elmenco
*C7, C12, C17	22 µF, 15 V, 20%	150D226X0015B2	Sprague
C18	0.0012 µF, 500 V	DM-19-122J	Arco-Elmenco
C19	0.027 µF, 150 V, 10%	617G27391, 5W2	Good-All
C20	0.0022 µF, 150 V, 10%	617G22291, 5W2	Good-All
C21	220 pF, 500 V	DM-15-221J	Arco-Elmenco
C22	68 pF, 500 V	DM-15-680J	Arco-Elmenco
*C23	4.7 µF, 35 V, 20%	150D475X0035B2	Sprague
C24	0.0012 µF, 500 V	DM-19-122J	Arco-Elmenco
C25 to C30	470 pF, 300 V	DM-15-471J	Arco-Elmenco
CR1 to CR7, CR10 to CR19	Silicon diode, 100 V, 250 mW	1N916	Fairchild
CR8	Zener diode, 3.6 V, 400 mW, 5%	1N747A	Motorola
CR9, CR24	Zener diode, 8.2 V, 400 mW, 5%	1N756A	Motorola
CR20, CR21	Silicon diode, 175 V, 500 mW	1N485B	Fairchild
CR22	Zener diode, 4.3 V, 400 mW, 5%	1N749A	Motorola
CR23	Zener diode, 15 V, 10 W, 5%	1N2979B	Motorola
Q1 to Q10, Q12 to Q15	Silicon transistor, 30 V, 800 mA	2N2222	Motorola
*Q11	Silicon transistor, 40 V, 600 mA	2N2904	Motorola
R1, R5	2370 Ω, $\frac{1}{2}$ W, 1%	MEC T-0	IRC
R2, R4	26 700 Ω, $\frac{1}{2}$ W, 1%	MEC T-0	IRC
R3	330 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R6, R7	22 000 Ω, $\frac{1}{2}$ W, 1%	MEC T-0	IRC
R8, R9, R37, R39	51 000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R10, R11, R19, R20, R28, R29, R56	1500 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R12, R13, R21, R22, R30, R31, R38	8200 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R14, R15, R23, R24, R32, R33	6800 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R16, R17, R25, R26, R34, R35, R40	22 100 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC

*Parts not on JPL Spec. ZPP-2061-PPL-F.

Figure 23. – Logic common to all
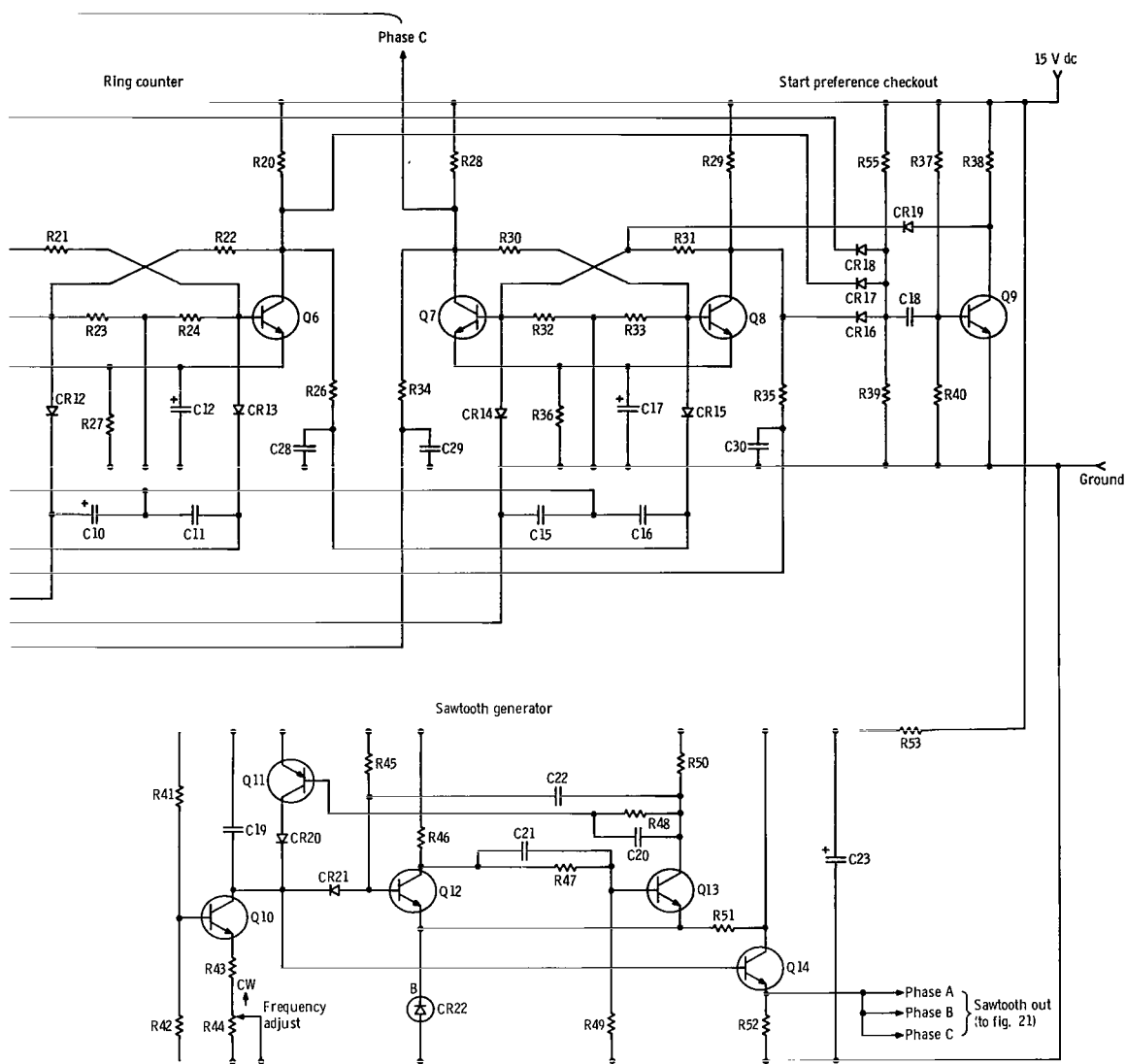
Reference designation	Description	Type or part number	Manufacturer
R18, R27, R36	220 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R41, R51, R57	2200 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R42, R43	1000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R44	5000 Ω pot, 1 W wire wound	3280W-1-502	Bourns
R45, R49	47 000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R46, R50	4700 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R47, R55	10 000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R48	3300 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R52	100 000 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R53	47 Ω, $\frac{1}{2}$ W, 5%	GBT-$\frac{1}{2}$	IRC
R54	330 Ω, 10 W, 1%	RHM-10	Dale

°Parts not on JPL Spec. ZPP-2061-PPL-F.

phases of PWM static inverter.

"The aeronautical and space activities of the United States shall be
conducted so as to contribute . . . to the expansion of human knowl-
edge of phenomena in the atmosphere and space. The Administration
shall provide for the widest practicable and appropriate dissemination
of information concerning its activities and the results thereof."

— NATIONAL AERONAUTICS AND SPACE ACT OF 1958

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